

REMARKS

Claims 1-8 are all the claims pending in the application. By this Amendment, Applicant amends claims 2-5. Claims 2-5 have been amended to correct minor, basic elements. Applicant respectfully submits that that they do not narrow the scope of the claim and do not raise any Festo implications.

The Examiner objected to the Drawings. In addition, claims 1-6 are rejected under 35 U.S.C. § 112, second paragraph and claims 1-7 are rejected under 35 U.S.C. § 102(e). Finally, the Examiner indicated that claim 8 is allowed.

I. Drawings

The Examiner objects to the drawings, asserting that Figure 1 should be labeled Prior Art. It is respectfully pointed out that Figure 1 filed on January 30, 2002, was labeled "Prior Art" as shown in the copy of the Drawings filed on January 30, 2002, which the Examiner will find attached. Accordingly, the Examiner is kindly requested to withdraw the objection and approve the formal drawings filed on January 30, 2002.

II. Claim Rejections under 35 U.S.C. § 112

The Examiner rejected claim 1-6 under section 112, second paragraph. The Examiner's pointing out, with particularity, of the aspects of the claim thought to be indefinite is gratefully noted. Specifically, the Examiner maintains that recitation "parallel to" is indefinite (see page 2 of the Office Action).

The Examiner has only provided reasons for rejecting claims 2-5. With respect to claims 1 and 6, they do not have the alleged indefinite recitation. Claims 1 and 6 do not recite any elements parallel to another element. As such, this rejection of claims 1 and 6 should be withdrawn. With respect to claims 2-5, Applicant respectfully requests the Examiner to withdraw this rejection in view of the self-explanatory claim amendments being made herein.

III. Claim Rejections under 35 U.S.C. § 102(e)

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,415,007 to Kawasumi ("hereinafter "Kawasumi"). Applicant respectfully traverses this rejection and respectfully requests the Examiner *to reconsider* this rejection in view of the comments, which follow.

Of these claims, only claim 1 is independent. Claim 1 requires:

an intermediate switch transistor is placed
between the drain node and the cascode
transistor...

The Examiner asserts that claim 1 is directed to a PLL charge pump and is anticipated by Kawasumi. The Examiner asserts that Kawasumi's p-channel MOS transistor (P6) and n-channel MOS transistor (N6) is equivalent to intermediate switch transistor, and p-channel MOS transistor (P7) and n-channel MOS transistor (N5) is equivalent to cascade transistor, as set forth in claim 1 (see pages 3-4 of the Office Action). The Examiner further maintains that although Kawasumi does not identify them as such, "the figures show the similarity to the Applicant's structure" (see page 4 of the Office Action).

Applicant respectfully disagrees with the Examiner. Applicant has carefully restudied Kawasumi's discussion of the charge pump with MOS transistors as well as the Figures, which do not teach or show a charge pump with an intermediate switch transistor and a cascode transistor as set forth in claim 1.

To begin, Applicant incorporates all arguments made in the previous amendment under 37 C.F.R. § 1.111 filed on June 10, 2003. Moreover, Applicant respectfully submits that there are essential differences between the switch transistor and a cascode transistor. For example, there is an essential functional difference between a cascode transistor and an intermediate switch transistor. The switching transistor is a transistor for switching on or off the current by offering a digital signal at the input of the switching transistor. A cascode transistor, however, is a transistor for establishing a certain current (bias current) through, for example, the transistor chain M2, M5 and M6, and for obtaining a constant voltage with a low variation at the drain-nodes A and B. At the input of such cascode transistor a certain fixed analogue voltage is supplied for setting the current at a certain bias-level. In short, a switching transistor switches on and off the current and receives a digital signal at the input, whereas a cascade transistor is maintaining a certain, stable flow of the current with a fixed analog voltage at the input.

Kawasumi teaches a charge pump in PLL 14 with a first and a second sub charge including common charging and discharging terminals and performing charging/discharging operations. If the first sub pump is charging, the second sub pump is discharging and visa versa (Fig 5; col. 9, lines 6 to 12). Each sub pump has a p-channel MOS transistor (hereinafter "p") and n-channel MOS transistor (hereinafter "n"), see Fig. 8; col. 9, lines 5 to 38. Injunction

capacitors, C1, C2, C3 and C4 are placed between transistors, p1 and p2, n2 and n3, p5 and p6, n6 and n7, respectively (col. 9, lines 28 to 32 and lines 61 to 65). When the charge pump 18 starts charging, the potential drain of p1 becomes operable after the accumulation of electricity in the capacitor C1. When the charge pump 18 starts discharging, the potential drain of p1, the potential drain of n3 becomes operable after the accumulation of electricity in the capacitor C2 (col. 10, line 62 to col. 11, line 19). In other words, the bias current is established by the capacitors. This is disadvantageous because the charging and discharging of the capacitor, causes a delay in switching on and off the current

In short, Kawasumi teaches only p MOS and n MOS transistors, which are field effect transistors, equivalent to each other in structure and functionality. The reference fails to teach or suggest a switch transistor and a cascode transistor as set forth in claim 1.

Therefore, an intermediate switch transistor is placed between the drain node and the cascode transistor as set forth in claim 1 is not suggested or taught by Kawasumi, which lacks an intermediate switch transistor and a cascode transistor. For at least these reasons, Applicant respectfully submits that independent claim 1 is patentably distinguishable from Kawasumi. Applicant, therefore, respectfully requests the Examiner *to reconsider* and withdraw this rejection of independent claim 1. Also, Applicant respectfully submits that claims 2-7 are allowable at least by virtue of their dependency on claim 1.

IV. Allowable Subject Matter

Applicant thanks the Examiner for allowing claim 8.

Amendment Under 37 C.F.R. § 1.116
U.S. Application No.: 10/058,804

Attorney Docket No.: Q68166

V. Conclusion and request for telephone interview.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

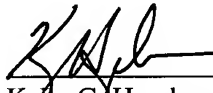
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